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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,164	11/25/2003	Cheng-Hsing Chien	11906-US-PA	1163

31561 7590 03/02/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,164	CHIEN ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 15 is objected to because following informalities:

line 2, replace "said rimming parameter" with – said trimming parameter --.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being unpatentable by Lesher (US Patent 6,396,759).

3. As to claim 1, 7 and 13 Lesher describes:

(1) An integrated circuit comprising:

a major circuit providing a major function (IC 100 includes circuit 140 that is capable of being trimmed) (col.2, ll.35-37; col.3, ll.37-42; Fig.1);

a trimming circuit being trimmable for adjusting (At least one fuse link is connectable to the circuit 140, by way of a fuse sense circuit 120, for trimming the circuit 140. The circuit 140 is trimmed by selectively opening (blowing) one or more of the fuses F1-F4- col.2, ll.45-51; fuse sense circuit 120 may be configured to identify whether there is a large current or no current coming from the fuses F1-F4 – col.2, ll.57-59) and fixing an electric characteristic of said integrated circuit (if the circuit 140 is a

voltage reference, then the fuses can be blown to match the first configuration of fuses, if they provide an acceptable voltage- col.4, ll.21-23) (col.1, ll.13-17; col.1, ll.56-67; col.2, ll.22-33; col.2, ll.45-60; col.3, ll.37-42; col.4, ll.21-23; col.5, ll.15-28);

a simulating device (register 110, Fig.1) simulating an operation of said trimming circuit and sending out a simulating signal to temporarily change said electric characteristic of said integrated circuit (during the trimming process, instead of blowing the trimming fuses, it is possible to enable a test function for example, by flipping a test function enable bit in a register--allowing the tester to duplicate the function of blowing the real fuse links. This capability essentially allows the tester to test the function of blowing the links. The test can be repeated, while changing the complement of (simulated) blown fuse links in the test function-col.2, ll.24-31; if the initial approximation does not produce an acceptable output from the circuit 140, then another configuration of test register bits 110a-110d may be written to the register 110, and the test can be repeated, until the output of the circuit 140 falls within the predetermined tolerance-col.4, ll.16-20) (col.2, ll.23-40; col.2, ll.61-67; col.3, ll.1-3; col.3, ll.37-42); and

a multiplexer having an output terminal, a plurality of input terminals, and a selection terminal (The first bit 110e of register 100 is provided to the select input of each multiplexer 130-133- col.3, ll.13-15), said output terminal being coupled to said major circuit, said plurality of input terminals being coupled to said trimming circuit and said simulating device (Each multiplexer 130-133 has a first data input connected to a respective one of the plurality of fuse links 150-153. Each multiplexer 130-133 has a second data input connected to a respective test data bit 110a-110d of the register 110-

col.3, ll.15-19; the fuse sense circuit 120 provides the output signal of the fuse links 150-153 to the multiplexers 130-133- col.3, ll.21-23) (col.3, ll.3-23; ; col.3, ll.37-42);

(7) An integrated circuit, said integrated circuit being simulated and trimmed in a testing system, said testing system including a testing device and a simulating device, said integrated circuit comprising (Abstract, Fig.1):

a major circuit providing a major function (IC 100 includes circuit 140 that is capable of being trimmed) (col.2, ll.35-37; col.3, ll.37-42; Fig.1);

a trimming circuit being trimmable for adjusting (At least one fuse link is connectable to the circuit 140, by way of a fuse sense circuit 120, for trimming the circuit 140. The circuit 140 is trimmed by selectively opening (blowing) one or more of the fuses F1-F4- col.2, ll.45-51; fuse sense circuit 120 may be configured to identify whether there is a large current or no current coming from the fuses F1-F4 – col.2, ll.57-59) and fixing an electric characteristic of said integrated circuit (if the circuit 140 is a voltage reference, then the fuses can be blown to match the first configuration of fuses, if they provide an acceptable voltage- col.4, ll.21-23) (col.1, ll.13-17; col.1, ll.56-67; col.2, ll.22-33; col.2, ll.45-60; col.3, ll.37-42; col.4, ll.21-23; col.5, ll.15-28);

a simulating device (register 110, Fig.1) simulating an operation of said trimming circuit and sending out a simulating signal to temporarily change said electric characteristic of said integrated circuit (during the trimming process, instead of blowing the trimming fuses, it is possible to enable a test function for example, by flipping a test function enable bit in a register--allowing the tester to duplicate the function of blowing the real fuse links. This capability essentially allows the tester to test the function of

blowing the links. The test can be repeated, while changing the complement of (simulated) blown fuse links in the test function-col.2, ll.24-31; if the initial approximation does not produce an acceptable output from the circuit 140, then another configuration of test register bits 110a-110d may be written to the register 110, and the test can be repeated, until the output of the circuit 140 falls within the predetermined tolerance-col.4, ll.16-20) (col.2, ll.23-40; col.2, ll.61-67; col.3, ll.1-3; col.3, ll.37-42); and

a multiplexer having an output terminal, a plurality of input terminals, and a selection terminal (The first bit 110e of register 100 is provided to the select input of each multiplexer 130-133- col.3, ll.13-15), said output terminal being coupled to said major circuit, said plurality of input terminals being coupled to said trimming circuit and said simulating device (Each multiplexer 130-133 has a first data input connected to a respective one of the plurality of fuse links 150-153. Each multiplexer 130-133 has a second data input connected to a respective test data bit 110a-110d of the register 110-col.3, ll.15-19; the fuse sense circuit 120 provides the output signal of the fuse links 150-153 to the multiplexers 130-133- col.3, ll.21-23) (col.3, ll.3-23; col.3, ll.37-42);

(13) A method for simulating and circuit, comprising:

detecting an electric characteristic of said integrated circuit (The circuit 140 is tested to obtain first test results with the fuses F1-F4 intact. The first test results are compared to a set of predetermined desired values –col.4, ll.6-9; the circuit 140 is a voltage reference- col.4, l.21);

obtaining a trimming parameter based on said electric characteristic of said integrated circuit (To initiate the test, the tester enables the test circuit 101 on the IC

100 by setting the contents of register 110. The first bit 110e is set to its enabled value (e.g., a "1"), and the other bits are set to a first approximation of the optimal trim value. For example, the first approximation may comprise values of the bits that would be produced by the conventional trim algorithm, based on the fabrication conditions –col.3, ll.60-67; if the circuit 140 is a voltage reference, then the fuses can be blown to match the first configuration of fuses, if they provide an acceptable voltage-col.4, ll.21-23) (col.3, ll.60-67; col.4, ll.21-23);

simulating a trimming operation to adjust said electric characteristic of said integrated circuit so that said electric characteristic of said integrated circuit is within an allowable range (If the initial approximation does not produce an acceptable output from the circuit 140, then another configuration of test register bits 110a-110d may be written to the register 110, and the test can be repeated, until the output of the circuit 140 falls within the predetermined tolerance- col.4, ll.16-20); and

trimming said integrated circuit based on said trimming parameter (trimming the circuit 140 of FIG. 1,... The first bit 110e is set to its enabled value (e.g., a "1"), and the other bits are set to a first approximation of the optimal trim value. For example, the first approximation may comprise values of the bits that would be produced by the conventional trim algorithm, based on the fabrication conditions) (col.3, ll.58-67; col.4, ll.11-15; col.4, ll.23-26).

4. As to claim 2-6, 8-12 and 14-15 Lesher recites:

(2), (3), (5), (8), (9), (15) The circuit/method, wherein said selection terminal of said multiplexer receives a selection signal to select one of said simulating device and said trimming circuit to connect said major circuit (col.3, ll.4-23; col.3, ll.37-57);

(4) The circuit, wherein said simulating signal is sent to said major circuit to temporarily change said electric characteristic of said integrated circuit (col.2, ll.23-40; col.2, ll.61-67; col.3, ll.1-3; col.3, ll.37-42);

(6), (11), (12) The circuit, wherein said electric characteristic of said integrated circuit being fixed after said trimming operation (col.1, ll.56-67; col.2, ll.22-33; col.4, ll.21-23);

(10) The circuit , wherein testing device detects said electric characteristic and obtains a trimming parameter (col.3, ll.60-67; col.4, ll.6-9; col.4, ll.21-23);

(14) The method of claim 13, wherein said integrated circuit includes a multiplexer, a trimming circuit, and a major circuit (col.1, ll.13-17; col.1, ll.56-67; col.2, ll.22-40; col.2, ll.35-37; col.2, ll.45-67; col.3, ll.1-23; col.3, ll.37-42; col.3, ll.58-67; Fig.1; col.4, ll.11-26; col.5, ll.15-28).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N L

THUAN DO
Primary examiner.
02/15/2006